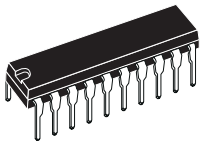
L6611

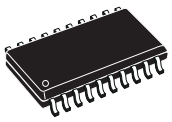
DIGITALLY PROGRAMMABLE SECONDARY HOUSEKEEPING CONTROLLER

- OV/UV DETECTION FOR 3.3V, +5V, ±12V RAILS AND 5V (OR 3.3V) AUX. VOLTAGE
- AC MAINS UV (BROWNOUT) DETECTION WITH HYSTERESIS
- ON-LINE DIGITAL TRIMMING FOR 5V/12V, 3.3V, 5V (OR 3.3V) AUX. FEEDBACK REFERENCES AND AC MAINS UV.
- DIGITALLY SELECTABLE OPTIONS
- ERROR AMPLIFIERS FOR 5V/12V RAILS (MAIN SUPPLY), 3V3 POST-REGULATOR (MAG_AMP OR LINEAR) AND AUXILIARY SUPPLY.
- MAIN SUPPLY ON/OFF CONTROL AND POWER GOOD SIGNAL
- 50mA CROWBAR DRIVE FOR AUXILIARY OUTPUT OVP.
- OPEN GROUND PROTECTION
- 8ms DIGITAL SOFT START
- 64 ms UV/OC BLANKING AT START-UP

BCD TECHNOLOGY



DIP20



SO20

ORDERING NUMBERS:

L6611N

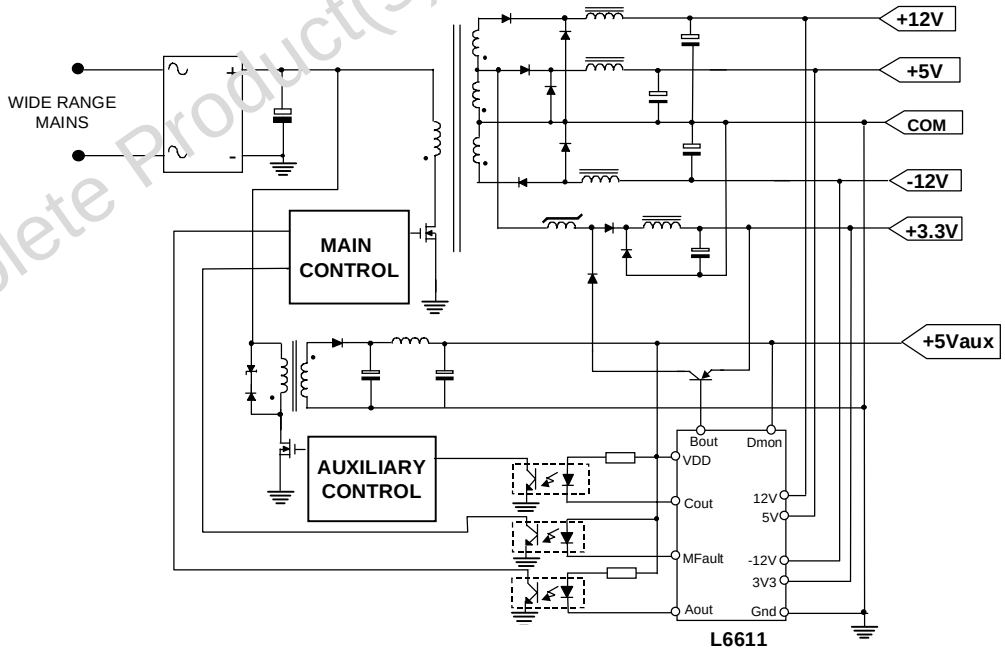
L6611D

L6611DTR(T & Reel)

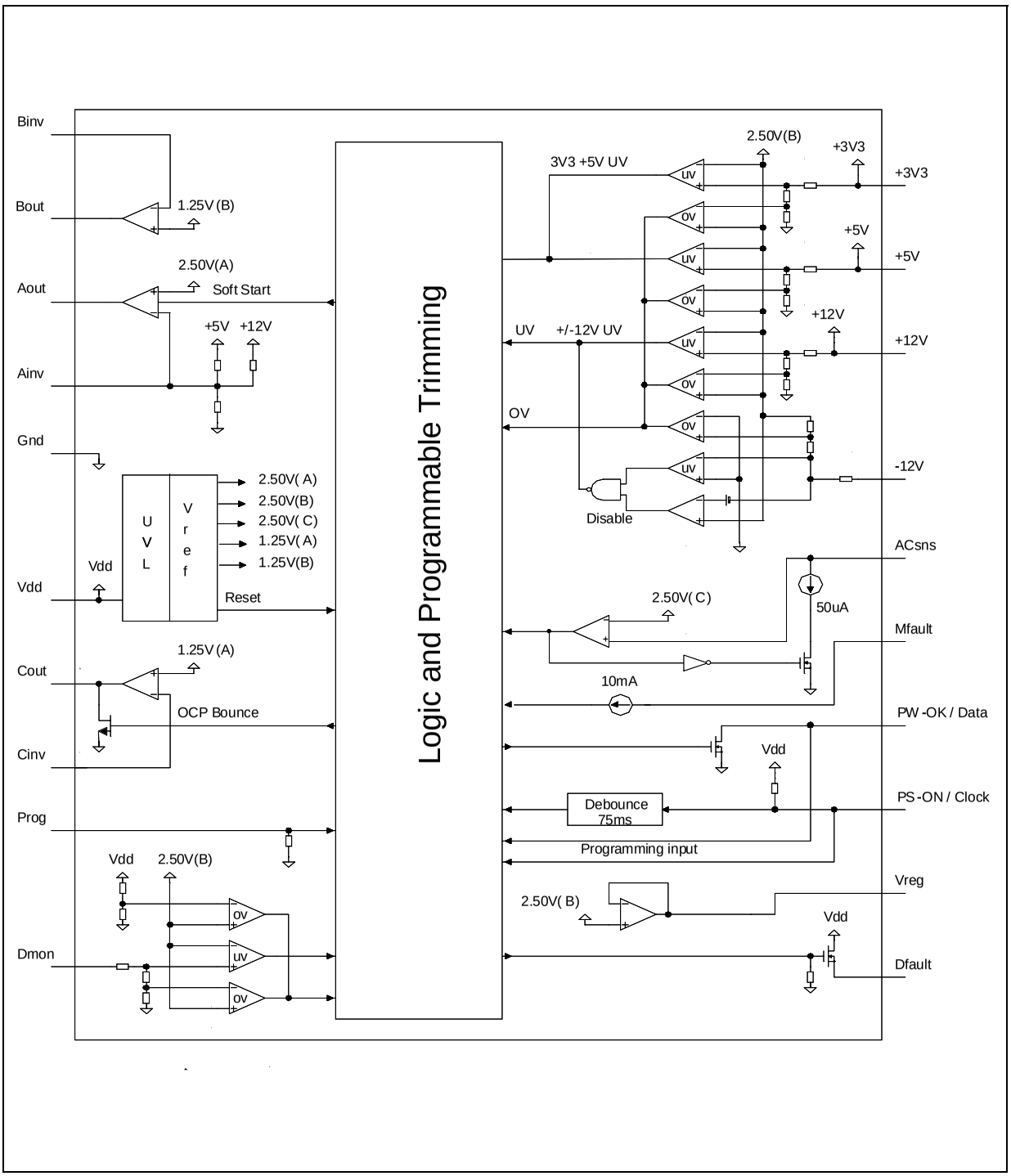
APPLICATIONS

- SWITCHING POWER SUPPLIES FOR DESKTOP PC'S, SERVERS AND WEB SERVERS
- SUPERVISOR FOR DISTRIBUTED POWER

TYPICAL APPLICATION CIRCUIT



BLOCK DIAGRAM



DESCRIPTION

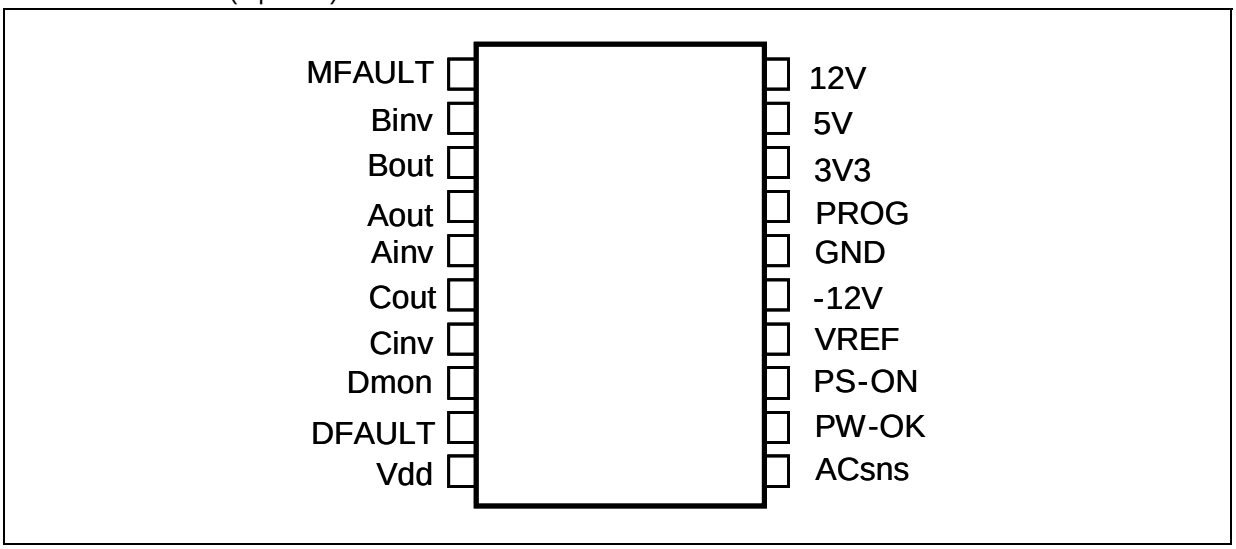
The L6611 is a control and housekeeping IC developed in BCD technology; it is intended for acting at the secondary side of desktop PC's or server's switching power supplies, in presence of standard voltage rails (+3.3V, +5V, ±12V) generated by a main converter and of a supply line generated by an auxiliary converter. The typical application circuit is showed on the front page.

The Housekeeping's main function is to control and monitor the voltages generated by both the main and the auxiliary converter: it senses those voltages, sends feedback signals to the primary controllers for regulation and, upon detection of an undervoltage (UV), or overvoltage (OV) condition, reports such fault and takes proper action to protect the system.

However, the peculiar feature of this IC is its digital programming capability that enables an accurate trimming of the output voltage rails during production test via software, without any use of external discrete trimming components or need for manual intervention on the PSU. It is also possible to program some of the monitoring functions and select how UV and OC conditions are handled in the main converter: whether latched-mode (the information is latched and released only by forcing the restart of the IC) or bouncing-mode (an attempt is made to automatically restart the converter after 1 second wait).

A key feature of this IC is its contribution to a very low external component count. Besides the extensive use of onboard programmable switches, which prevents the need for external trimming components, the IC embeds reference voltages, error amplifiers and most of the housekeeping circuitry normally required.

PIN CONNECTION (top view)



PIN DESCRIPTION

Pin #	Name	Description
1	**MFAULT**	Main converter on/off control. This pin is a 10mA current sink used for driving an opto-isolator. It is normally low when PS-ON (#13) is pulled low. If a fault is detected or PS-ON goes high, this pin goes high too. To allow power up, the functions are digitally blanked out for a period (UVB function) and MFAULT (#1) stays low. There is no delay for the OV protection function.
2	**Binv**	Inverting input to the error amplifier for the 3V3 post-regulator (either mag-amp or linear). The non-inverting input is connected to an internal 1.25V reference that can be digitally trimmed.
3	**Bout**	Output of the 3V3 error amplifier. It typically drives either a PNP transistor that sets the mag-amp core or the pass element of a linear regulator. Also node for error amplifier compensation. The maximum positive level of this output is clamped at about 3.5V to improve response time. Large signal slew rate is limited to reduce noise sensitivity.

PIN DESCRIPTION (continued)

Pin #	Name	Description
4	**Aout**	Output of the error amplifier for the main converter. This pin typically drives an optocoupler and is also used for compensation along with Ainv (pin #5).
5	**Ainv**	Main loop error amplifier inverting input. The non-inverting input is connected to an internal 2.5V reference that can be digitally trimmed. A high impedance internal divider from +12V and +5V UV/OV sense pins (#19, #20) eliminates the need for external divider in most applications. The pin is used for error amplifier compensation.
6	**Cout**	Auxiliary loop optocoupler drive. Also node for error amp compensation. Large signal slew rate is limited to reduce sensitivity to switching noise.
7	**Cinv**	Inverting input for Auxiliary error amplifier. The non-inverting input is connected to an internal 1.25V reference that can be digitally trimmed.
8	**Dmon**	Dual or Auxiliary UV/OV monitor, Dmon is programmable to monitor 3V3 or 5V. To allow a correct power up, the UV function on this pin is blanked out during initial start-up. There is no delay for the OV function.
9	**DFAULT**	Dual or Auxiliary fault protection. When Dmon (#8) recognizes an over voltage, DFAULT and MFAULT (#1) go high. DFAULT is capable of sourcing up to 50mA. Possible applications are a crowbar across the Auxiliary output or an opto-coupled fault signal to the primary side.
10	**Vdd**	Positive input supply voltage. Vdd is normally supplied from the Auxiliary power supply output voltage. If Vdd-UVL detects a sustained under voltage, PW-OK (#12) will be pulled low and sending MFAULT (#1) high will disable the main converter.
11	**ACsns**	Analog of bulk voltage for AC fail warning. The usual source of this analog pin is one of the secondary windings of the main transformer. Hysteresis is provided through a trimmable 50µA current sink on this pin that is activated as the voltage at the pin falls below the internal reference (2.5V).
12	**PW-OK /Data**	Power good signal for the Main converter. When asserted high, this pin indicates that the voltages monitored are above their UV limits. There will be typically 250ms delay from the Main outputs becoming good and PW-OK being asserted. This is nominally an open drain signal. To improve robustness, this output has a limited current sink capability. In programming mode, this pin is used for data input; then the absolute maximum rating will be Vdd+0.5V.
13	**PS-ON / Clock**	Control pin to enable the Main converter. This pin has debouncing logic. A recognized high value on this pin will cause PW-OK (#12) to go immediately low and, after a delay of 2.5ms, to shut down the main PWM by allowing MFAULT (#1) to go high. During normal operation (or if not used) this pin has to be connected to a voltage lower than 0.8V. In programming mode, this pin will be used to clock serial data into the chip.
14	**VREF**	2.5V reference for external applications. This is a buffered pin. Shorting this pin to ground or to Vdd (#10) will not affect integrity of control or monitor references. An external capacitor (max. 100nF) is required whenever the pin is loaded (up to 5 mA), otherwise it can be left floating.
15	**-12V**	-12V UV/OV monitor. If connected to a voltage greater than 1.5V (e.g. VREF, #14), the function will be disabled.
16	**GND**	Ground pin. The connection integrity of this pin is constantly monitored and in case of either a bond wire or a PCB trace going open, MFAULT (#1) and DFAULT (#9) will be forced high switching off the supply.
17	**PROG**	The chip has 2 operating modes, depending on PROG input pin biasing: – *normal mode*: PROG should be floating or shorted to ground; – *programming mode*: forcing PROG high (+5V), the chip enters programming mode. PW_OK (#12) and PS_ON (#13) pins are disconnected from their normal functionality and they become inputs for DATA and CLOCK allowing the chip to be programmed. The programming mode allows selecting some options and adjusting some setpoints;

PIN DESCRIPTION (continued)

Pin #	Name	Description
18	**3V3**	3V3 UV/OV monitor. It uses a separate reference to the feedback reference.
19	**5V**	Input pin for 5V feedback, 5V current sense and 5V UV/OV monitor. 5V UV/OV uses a reference separate from that used for feedback. This pin connects the 5V part of the Main error amplifier feedback divider.
20	**12V**	Input pin for 12V feedback, 12V current sense and 12V UV/OV monitor.12V UV/OV uses a reference separate from that used for feedback. This pin connects the 12V part of the Main error amplifier feedback divider.

FUNCTION DESCRIPTION

Name	Description
OVP	Whenever one of the Main output voltages is detected going above its own OVP threshold, this function set MFAULT (#1) high latching the outputs off. The latch is released after cycling PS-ON (#13) switch or by reducing Vdd (#10) below the UV threshold.
UVP	Whenever one of the Main output voltages is detected going under its own UVP threshold, this function sets MFAULT (#1) high; if latch mode has been selected, this function will be latched. Otherwise an attempt will be made to restart the device after 1 second delay. If ACsns (#11) is low due to a brownout condition, UVP is disabled.
UVB	Undervoltage blanking. When either converter is enabled, the relevant UV/OC monitoring circuits must not intervene to allow all outputs to come within tolerance. 64 ms timing is provided; for the auxiliary converter the timing starts as the IC has a valid supply, for the main converter it starts as the ACsns pin detects a valid input voltage for the converter.
PW-OK delay	PW-OK delay. After power-up, when the all of the monitored voltages are above their own UV threshold the PW-OK pin (#12) will be kept low for additional 250ms (typ.) to make sure all the outputs are settled.
OFF delay	Power-off delay. As soon as PS-ON (#13) pin is recognized high, indicating an imminent turn-off condition, PW-OK (#12) pin will go low immediately . The converter will be turned off after a delay of 2.5ms.
Debounce	The PS-ON signal input has debounce logic to prevent improper activation. All of the monitored inputs have digital filtering/debounce logic on board for high noise immunity.
AC-hysteresis	AC sense hysteresis. Programmable hysteresis is provided on the ACsns input (#11) to avoid undesired shutdown caused by noise as the voltage at the pin is near the threshold or by the voltage ripple across the bulk capacitor.
Vdd-OVP	Vdd is monitored for overvoltage. If an overvoltage is detected, MFAULT (#1) and DFAULT (#9) are latched high.
Vdd-UVL	To prevent false signals of any of IC's output pins, an under voltage lock-out circuit monitors Vdd and keeps all IC's output at their default OFF level until Vdd reaches a sufficient minimum voltage for ensuring integrity. When Vdd goes below the UV threshold, all latches are reset and volatile programming memory cleared.
Dual-OVP	Dmon (#8) is monitored to detect an overvoltage condition; in this case MFAULT (#1) and DFAULT (#9) are latched high.
Dual-UVP	Dmon (#8) is monitored to detect an undervoltage condition; in this case MFAULT (#1) is latched high and Cout (#6) is pulled low.

FUNCTION DESCRIPTION (continued)

Name	Description
Soft-start	The IC provides an on-board 8ms soft-start, a quasi-monotonic ramp from 0V to 2.5V for the A error amplifier reference voltage, in order to avoid high current peaks in the primary circuit and output voltage overshoots at start-up. In fact, if this reference gets the nominal value as soon as the power-up occurs, the A E/A will go out of regulation and tend to sink much more current, thus forcing PWM to work with the maximum duty-cycle.
Bounce or Latch-mode	This option allows setting either latched-mode or auto restart after 1 second delay in case of undervoltage faults.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vdd	Supply voltage	-0.5 to +7	V
	Voltage on PROG, PS-ON/Clock, DFAULT, VREF, and error amplifier pins	-0.5 to Vdd+0.5	V
	Voltage on MFAULT, PW-OK, Dmon and positive UV, OV, OC, AC sense pins.	-0.5 to +16	V
	Voltage on and -12V UV/OV sense pin	-16 to +5	V
	Maximum current in ESD clamp diodes	10	mA
T_J	Operating Junction Temperature	-25 to 150	°C
T_{STO}	Storage Temperature	-50 to 150	°C
T_L	Lead Temperature (soldering, 10 seconds)	300	°C

THERMAL DATA

Symbol	Parameter	DIP20	SO20	Unit
$R_{th\ j\text{-}amb}$	Max. Thermal Resistance junction-to-ambient (*)	70	120	°C/W

(*) mounted on board

ELECTRICAL CHARACTERISTCS

(unless otherwise specified: T_J = 0 to 105°C; V_{DD} = 5V, V_{3V3} = 3.3V, V_{5V} = 5V, V_{-12V} = -12V, , V_{Dmon} = V_{DD}, PS-ON = low)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION						
$V_{DD(ON)}$	Start-up threshold		4.2	4.3	4.6	V
$V_{DD(OFF)}$	Minimum operating voltage after turn-on		3.7	3.8	4.1	V
$V_{DD(H)}$	Hysteresis		0.25	0.5	0.75	V
V_{DDOV}	Vdd overvoltage		6.1	6.3	6.8	V
I_{DD-ON}	Operating supply current	No Fault		5	7	mA
FAULT THRESHOLDS						
Vout = 3.3V						
UV	3V3 undervoltage		2.80	2.90	3.00	V
OV	3V3 overvoltage		4.00	4.15	4.30	V
	3V3 bias current			50	65	µA
Vout = 12V						
UV	12V undervoltage		10.60	10.80	11.00	V
OV	12V overvoltage		13.50	14.00	14.50	V
	12V bias current			100	130	µA
Vout = -12V						
UV	-12V undervoltage		-9.00	-9.50	-10.0	V
OV	-12V overvoltage		-14.4	-15.0	-15.6	V
V_D	-12V disable voltage	Voltage to disable comparator	1.3	1.5	1.7	V
	-12V bias current		-65	-50		µA
Vout = 3.3V Aux/Dual (Dmon option)						
UV	3V3 undervoltage		2.80	2.90	3.00	V
OV	3V3 overvoltage		4.00	4.15	4.30	V
Vout = 5V Aux/Dual (Dmon option)						
UV	5V undervoltage		4.25	4.40	4.55	V
OV	5V overvoltage		6.00	6.25	6.50	V
	Bias current			50	65	µA
ACsense / Hysteresis						
	Bias current	V_{ACsns} = 2.7V		5	10	µA

ELECTRICAL CHARACTERISTCS (continued)
(unless otherwise specified: T_J = 0 to 105°C; V_{DD} = 5V, V_{3V3} = 3.3V, V_{5V} = 5V, V_{-12V} = -12V, , V_{Dmon} = V_{DD}, PS-ON = low)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
UV	AC undervoltage		2.375	2.50	2.625	V
	Trim range		-5		+5	%
	Trim resolution			0.64		%
I_{ACH}	Hysteresis current		20	50	80	µA
	Hysteresis trim range		-20		+20	%
H_S	Hysteresis adjust step			5		%
FAULT OUTPUTS						
V_{POKH}	PW-OK high state	No faults	3			V
V_{POKL}	PW-OK low state	I_{SINK} = 15mA			0.4	V
I_L	MFAULT high state leakage	PS-ON = high			1	µA
MF_{ISNK}	MFAULT sink current	PS-ON = low, V_{MFAULT} = 4V	6	10	15	mA
	MFAULT OV debounce	Minimum OV pulse before MFAULT is latched.	4	6	8	µs
	MFAULT debounce ±12V UV	Minimum UV pulse before MFAULT is latched.	4	6	8	µs
	MFAULT debounce +5V, 3V3, UV	Minimum UV pulse before MFAULT is latched.	250	450	650	µs
DF_{IOH}	DFAULT output high source current	Overvoltage condition V_{DFAULT} = 1.5V	-25	-50	-95	mA
D_{FVOH}	DFAULT output high voltage	I_{DFAULT} = 0mA, T_{amb} = 25°C, Overvoltage condition	2.1	2.4	2.7	V
V_{OUT}	DFAULT output low voltage	I_{DFAULT} = 1mA, no faults	0.3	0.5	0.7	V
	DFAULT OV debounce	Minimum OV pulse before DFAULT is latched.	4	6	8	µs
	DFAULT UV debounce	Minimum UV pulse before DFAULT is latched.	250	450	650	µs
START-UP / SHUTDOWN FUNCTIONS						
t5	DFAULT UV blanking delay	Delay from V_{DD}(on) to DFAULT UV active.	44	64	84	ms
t1	MFAULT UV blanking delay	Delay from AC_{SNS} high to Main UV active	44	64	84	ms
t2	PW-OK blanking delay	Main's UV good to PW-OK high	175	250	325	ms
t4 (t_{DELAY})	PS-ON delay time	Delay from PS-ON input to MFAULT	1.75	2.5	3.25	ms

ELECTRICAL CHARACTERISTCS (continued)
(unless otherwise specified: T_J = 0 to 105°C; V_{DD} = 5V, V_{3V3} = 3.3V, V_{5V} = 5V, V_{-12V} = -12V, , V_{Dmon} = V_{DD}, PS-ON = low)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	PS-ON Input High Voltage	I_{IN} = -200µA	2.0			V
V_{IL}	PS-ON Input Low Voltage				0.8	V
	PS-ON Input high clamp	I_{PS-ON} = 100 µA		Vdd +0.7		V
R_{PS-ON}	PS-ON Pull-up to V_{DD}	V_{PS-ON} = 0V	25	50	100	KΩ
t3	PS-ON debounce	PS-ON input minimum pulse width for a valid logic change.	50	75	100	ms
t_{SS}	Error Amp. A Soft-Start period	VFB quasi-monothonic ramp from 0 to 2.5V		8		ms
V_{STEP}	Soft Start Step	Ramp 0V to 2.5V		39		mV
VOLTAGE REFERENCE (BUFFERED EXTERNAL PIN)						
V_{REF}	Output Voltage	I_{REF} = 1 - 5 mA; C_{REF} = 47nF	2.375	2.50	2.625	V
I_{SC}	Short circuit current	V_{REF} = 0		10	20	mA
MAIN CONVERTER FEEDBACK (ERROR AMPLIFIER A)						
V_{FB}	Input Voltage	T_j = 25° C	2.375	2.50	2.625	V
	Trim Range	About nominal	-5		+5	%
	Trim resolution			0.64		%
Z_{FB}	Divider impedance	from Ainv to GND. 5V and 12V connected to GND.	35	50	65	kΩ
	Temperature coefficient			26		Ω/°C
W_5	Divider 5/12 weighting	5V contribution to 5/12 feedback	47	50	53	%
A_{VOL}	Voltage gain	2V<V_{OUT}<4V	65			dB
GBW	Unity gain bandwidth			3		MHz
PSRR	Power supply rejection ratio	4.5V<V_{DD}<6V	60	70		dB
I_{OUTL}	Output sink current	V_{FB} = 2.7V, V_{OUT} = 1.1V	2	5	8	mA
I_{OUTH}	Output source current	V_{FB} = 2.3V, V_{OUT} = 4V	-1.0	-1.5	-2.0	mA
V_{OUTH}	Output high level	V_{FB} = 2.3V, I_{SOURCE} = 1 mA	4	4.5		V
V_{OUTL}	Output low level	V_{FB} = 2.7V, I_{SINK} = 2 mA		0.7	1.1	V
MAGAMP OR LINEAR POST-REGULATOR FEEDBACK (ERROR AMPLIFIER B)						
V_{FB}	Input Voltage	T_j = 25° C	1.22	1.25	1.28	V
	Trim Range	About nominal	-5		+5	%

ELECTRICAL CHARACTERISTCS (continued)
(unless otherwise specified: T_J = 0 to 105°C; V_{DD} = 5V, V_{3V3} = 3.3V, V_{5V} = 5V, V_{-12V} = -12V, , V_{Dmon} = V_{DD}, PS-ON = low)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Trim resolution			0.64		%
I_{BIAS}	Input bias current			-0.1	-1	µA
A_{VOL}	Voltage gain	2V<V_{OUT}<4V	65			dB
GBW	Unity gain bandwidth			3		MHz
PSRR	Power supply rejection ratio	4.5V<V_{DD}<6V	60	70		dB
I_{OUTL}	Output sink current	V_{FB} = 1.4V, V_{OUT} = 1.1V	2	5	8	mA
I_{OUTH}	Output source current	V_{FB} = 1.1V, V_{OUT} = 3V	-1.0	-1.5	-2.0	mA
V_{OUTH}	Output high level	V_{FB} = 1.1V, I_{SOURCE} = 1 mA	3	3.6	4	V
V_{OUTL}	Output low level	V_{FB} = 1.4V, I_{SINK} = 2 mA		0.7	1.1	V
AUXILIARY CONVERTER FEEDBACK (ERROR AMPLIFIER C)						
V_{FB}	Input Voltage	T_{amb} = 25° C	1.22	1.25	1.28	V
	Trim Range	About nominal	-5		+5	%
	Trim resolution			0.64		%
I_{BIAS}	Input bias current			-0.1	-1	µA
A_{VOL}	Voltage gain	2V<V_{OUT}<4V	65			dB
GBW	Unity gain bandwidth			3		MHz
PSRR	Power supply rejection ratio	4.5V<V_{DD}<6V	60	70		dB
I_{OUTL}	Output sink current	V_{FB} = 1.4V, V_{OUT} = 1.1V	2	5	8	mA
I_{OUTH}	Output source current	V_{FB} = 1.1V, V_{OUT} = 4V	-1.0	-1.5	-2.0	mA
V_{OUTH}	Output high level	V_{FB} = 1.1V, I_{SOURCE} = 1 mA	4	4.5		V
V_{OUTL}	Output low level	V_{FB} = 1.4V, I_{SINK} = 2 mA		0.7	1.1	V
V_{OUTL}	Output low level	Dmon = 2.7V, I_{SINK} = 5 mA			0.25	V
PROGRAMMING FUNCTIONS						
V_{PROGLO}	Prog Input Low				1.5	V
V_{PROGHI}	Prog Input High		3.5			V
R_{PROG}	Prog Pull Down			100		KΩ
$V_{CLOCKLO}$	Clock Input Low				0.8	V
$V_{CLOCKHI}$	Clock Input High		2			V

ELECTRICAL CHARACTERISTCS (continued)
(unless otherwise specified: T_J = 0 to 105°C; V_{DD} = 5V, V_{3V3} = 3.3V, V_{5V} = 5V, V_{-12V} = -12V, , V_{Dmon} = V_{DD}, PS-ON = low)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{CLOCK}	Clock Frequency				0.8	MHz
V_{DATALO}	Data Input Low				1.5	V
V_{DATAHI}	Data Input High		2			V
I_{FUSE}	PROM Fuse Current			400		mA
t_{FUSE}	PROM Fusing Time			3		ms

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. Supply start-up, UV and OV

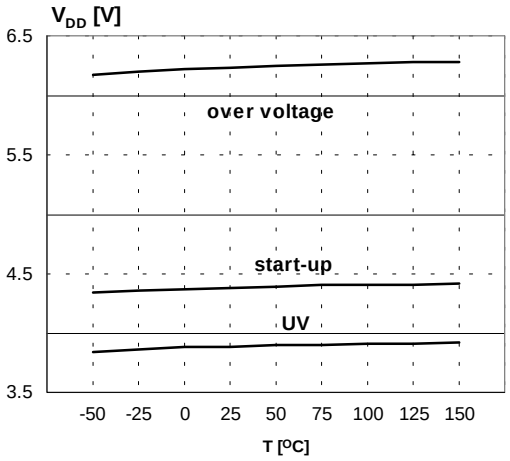


Figure 2. IC Supply current vs. supply voltage

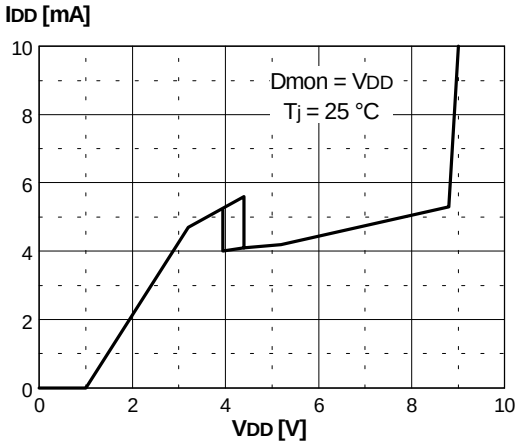


Figure 3. IC Supply current

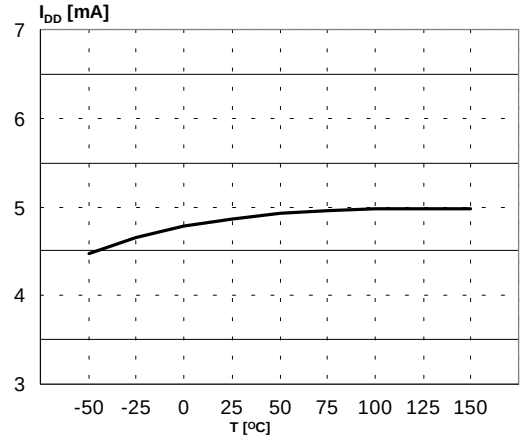


Figure 4. Monitored inputs bias current

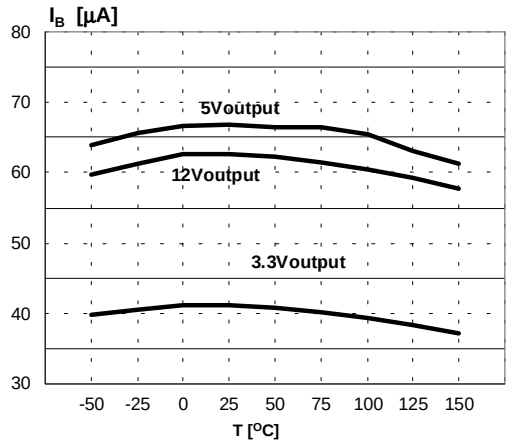


Figure 5. 3.3V fault thresholds

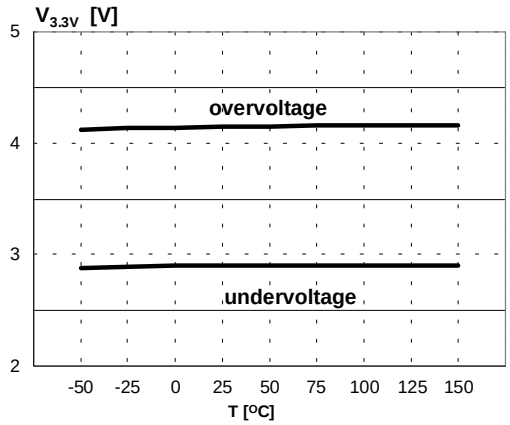
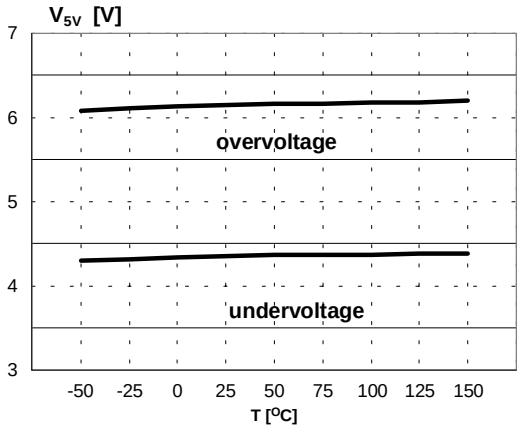


Figure 6. 5V fault thresholds



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

Figure 7. 12V fault thresholds

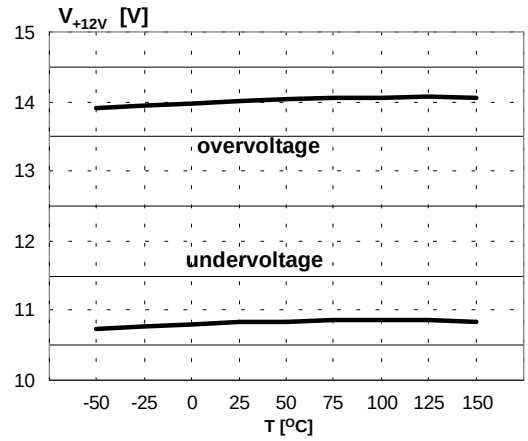


Figure 8. 3.3V/5V Dmon fault thresholds

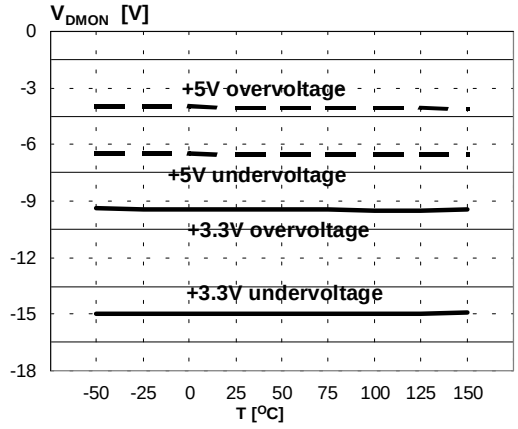


Figure 9. -12V bias current

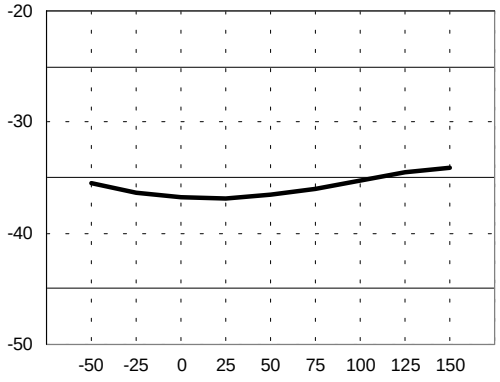


Figure 10. -12V fault thresholds

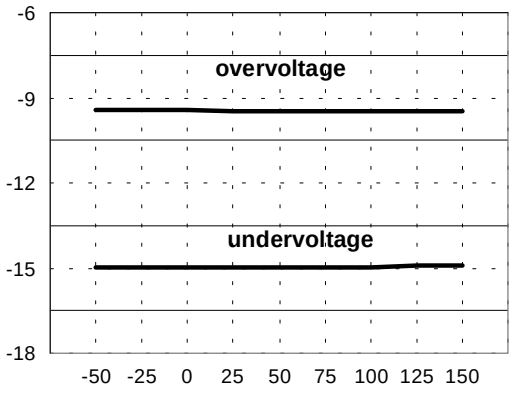


Figure 11. ACsense and external voltage references

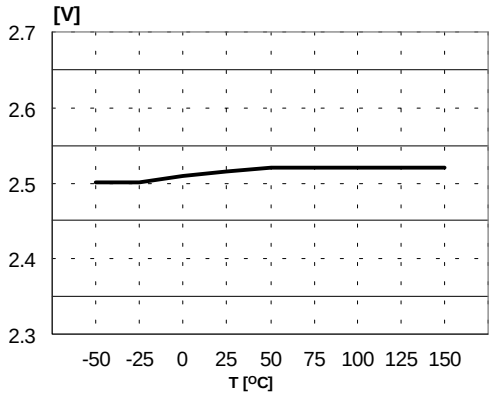
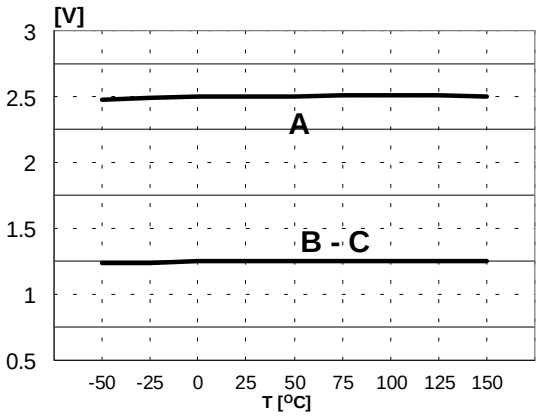
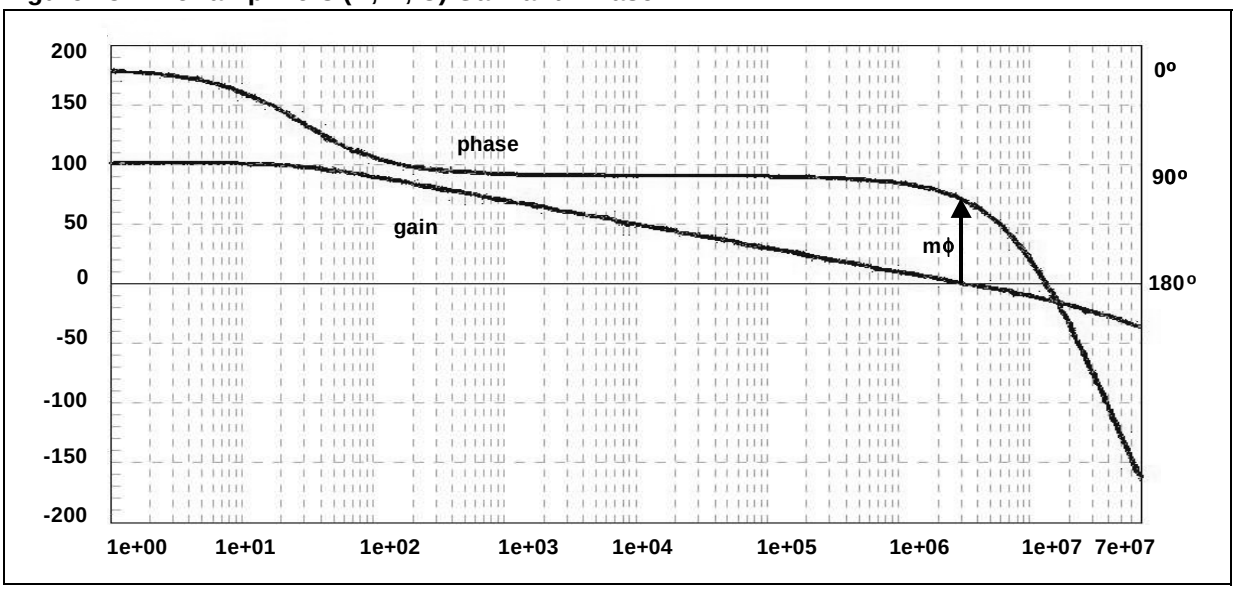


Figure 12. Error amplifier A, B and C reference voltage



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

Figure 13. Error amplifiers (A, B, C) Gain and Phase



APPLICATION INFORMATION INDEX

APPLICATION INFORMATION

1 ONBOARD DIGITAL TRIMMING AND MODE SELECTION

By forcing the PROG input pin high, the chip enters programming mode: the multifunction pins PW_OK and PS_ON are then disconnected from their normal functions (output pins) and are connected to internal logic as DATA and CLOCK inputs respectively, allowing chip programming even when the device is assembled on the application board. Onboard chip programming allows:

– selecting some working options;

– reference voltage setpoints adjusting.

It is also possible to verify the expected results before programming the chip definitively, in first instance, data can be loaded into a re-writeble volatile memory (a flip-flop array) where they are kept as long as the chip is supplied and can be changed as many times as one desires. A further operation is necessary to confirm the loaded data and permanently store them into a PROM (a poly-fuse array) inside the IC.

Several steps compose the trimming/programming process:

1. PROG pin is forced high;
2. a clock signal is sent to the PS-ON/clock pin;
3. a byte with the following structure:

MSB							**LSB**
D3	D2	D1	D0	A3	A2	A1	A0
Data				**Address**			

is serially sent to the PW-OK/DATA pin and loaded into the IC's volatile memory bit by bit on the falling edges of the clock signal (see Fig. 14); "Address" is the identification code of the parameter that has to be trimmed and "Data" contains the tuning bits;

4. PROG pin is forced low (warning: Vdd must never fall below V_{ddUVL0} during this process otherwise the contents of the volatile memory will be lost) and the result of the previous step is checked;
5. after any iterations of the steps 1-4 that might be necessary to achieve the desired value, force PROG pin high and send the following burn code

MSB							**LSB**
0	0	0	0	1	1	1	1

to permanently store the data in the PROM memory.

Table 1 shows the list of the 6 programmable classes of functions, each one identified by a different code A0..A3, and the corresponding trimmable parameter(s); in table 2 it is possible to find the trim coding for the E/A reference setpoints and in table 3 all the selections mode option coding are showed. The timing diagram of fig. 14 shows the details of data acquisition.

Table 1. Programmable functions

Address	Parameter(s)	Default value	Tuning bits
0001	Error amplifier A threshold	2.50V	D_3 D_2 D_1 D_O
0010	Error amplifier B threshold	1.25V	D_3 D_2 D_1 D_O
0011	Error amplifier C threshold	1.25V	D_3 D_2 D_1 D_O
0100	AC sense threshold	2.50V	D_3 D_2 D_1 D_O
0101	AC sense hysteresis	50µA	D_2 D_1 D_O
	Latch/Bounce mode selection	Latch mode	D_3
0110	Enable/Disable 12V UV/OV function	Enabled	D_3
	Enable/Disable 5V UV/OV function	Enabled	D_2
	5V/3V3 Dmon selection	5V selection	D_1
			don't care

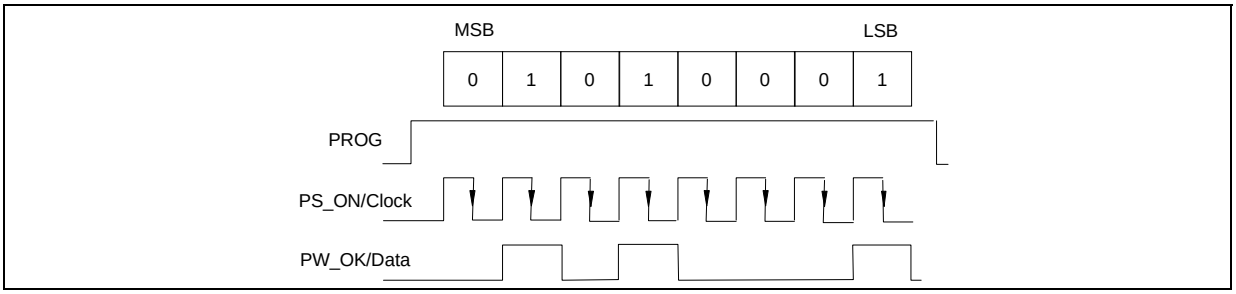
Table 2. Trim Coding

Parameter	E/A A threshold 2.5V typ.	E/A B threshold 1.25V typ.	E/A C threshold 1.25V typ.	ACsns threshold 2.5V typ.	ACsns Hysteresys 50µA typ.
Address	**0001**	**0010**	**0011**	**0010**	**0101**
Tuning Bits D_3 D_2 D_1 D_0	D3 D2 D1 D0 ΔV [mV]	D3 D2 D1 D0 ΔV [mV]	D3 D2 D1 D0 ΔV [mV]	D3 D2 D1 D0 ΔV [mV]	D2 D1 D0 ΔI [µA]
0 1 1 1	+112	+56	+56	+112	
0 1 1 0	+96	+48	+48	+96	
0 1 0 1	+80	+40	+40	+80	
0 1 0 0	+64	+32	+32	+64	
0 0 1 1	+48	+24	+24	+48	+7.5
0 0 1 0	+32	+16	+16	+32	+5.0
0 0 0 1	+16	+8	+8	+16	+2.5
0 0 0 0	0	0	0	0	0
1 1 1 1	-16	-8	-8	-16	-2.5
1 1 1 0	-32	-16	-16	-32	-5.0
1 1 0 1	-48	-24	-24	-48	-7.5
1 1 0 0	-64	-32	-32	-64	-10
1 0 1 1	-80	-40	-40	-80	
1 0 1 0	-96	-48	-48	-96	
1 0 0 1	-112	-56	-56	-112	
1 0 0 0	-128	-64	-64	-128	

Table 3. Mode coding

Parameter	Bounce or Latch Mode	Enable/Disable 12V UV/OV	Enable/Disable 5V UV/OV	5V/ 3.3V Dmon Selection
Address	**A3 A2 A1 A0 0101**	**A3 A2 A1 A0 0110**		
Bit Value	**Tuning Bit**			
	D3	**D3**	**D2**	**D1**
0	Latch	Enabled	Enabled	5V
1	Bounce	Disabled	Disabled	3.3V

Figure 14. Trimming/programming procedure: timing diagram



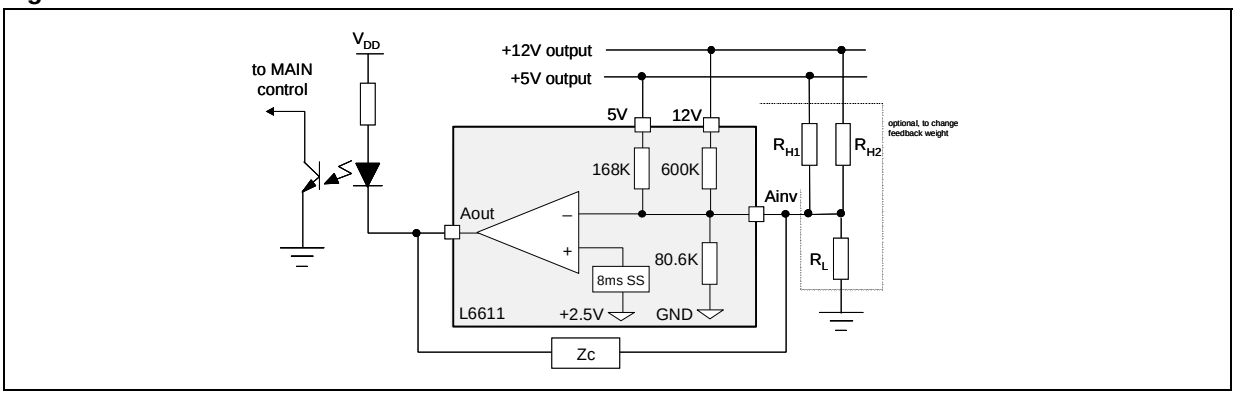
2 ERROR AMPLIFIERS AND REFERENCE VOLTAGES

Three error amplifiers are implemented on the IC to achieve regulation of the output voltages: a brief description follows for each section.

– **Main section: error amplifier A and Soft-Start.**
The circuit is designed to directly control the Main primary PWM through an optocoupler, providing very good regulation and galvanic isolation from the primary side. Typical solutions require a shunt regulator, like the TL431, as a reference and feedback amplifier to sense the output voltage and generate a corresponding error voltage; this voltage is then converted in a current transferred to the primary side through the optocoupler.
The feedback E/A amplifier is integrated in the IC: its non-inverting input is connected to an internally generated voltage reference, whose default value is typically 2.5V. It can however be trimmed to obtain a better precision (see "On board trimming and mode operating" section). Then, no TL431 is needed.
The E/A inverting input (Ainv, pin#5) and the E/A output (Aout, pin#4) are externally available and the frequency compensation network (Zc) will be connected between them (see fig. 15).
The high impedance (in the hundred kΩ) internal divider from 12V and 5V UV/OV sense pins eliminates the need for an external one in most applications, allowing a further reduction in the number of external component.
Under closed loop condition, the two upper branches, connected to 12V and 5V pins, supply equally the current flowing through R3= 80.6K (equal to 2.5V/R3).
In order to avoid high current peaks in the primary circuit and output voltage overshoots at start-up, the IC provides an on-board 8ms soft-start, a quasi-monotonic ramp from 0V to 2.5V for the A error amplifier reference voltage,. In fact, if this reference gets the nominal value as soon as the power-up occurs, the A E/A will go out of regulation and tend to sink much more current, thus forcing PWM to work with the maximum duty-cycle.

– **E/A and references voltage**
Being the inverting input of E/A externally available, it is possible to change the "weight" of the two contributions or even eliminate one of them by connecting external resistors of much lower value (R_L, R_{H1} and/or R_{H2} in fig. 15) that bypass the internal ones appropriately.
For example using R_L=2.4K, R_{H1}=3.9K and R_{H2}=24K, then the ratio between +5V and +12V output weight will be equal to 6:4.
By simply making R_{H1} = R_L (for example 2.4K) with no R_{H2}, only the +5V output is kept under feedback because the contribution of +12V branch (through the internal 600K resistor) will be negligible.
The pin #24 (12V) has to be connected to +12V output to guarantee the OV/UV monitoring.

Figure 15. Main feedback section



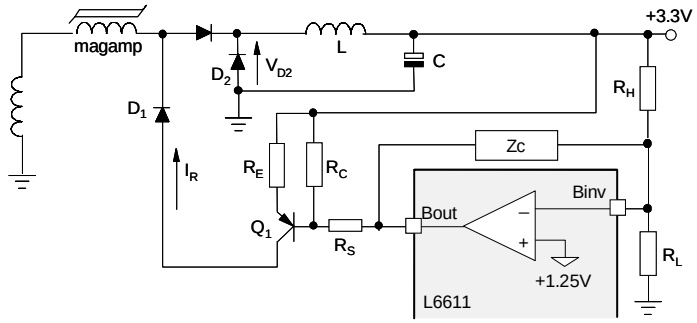
– **3.3V section, error amplifier B.**
It is the error amplifier used to set the magamp core through an external circuitry (see a typical schematic in figure 16).
The non-inverting input of the error amplifier is connected to a trimmable 1.25V internal voltage reference (see "On board trimming and mode operating" paragraph). The E/A inverting input is externally available (Binv, pin#2) and is connected to the output divider (R_H and R_L); the output pin (Bout,

pin#3) drives the external circuitry that biases the magamp core. Between these pins it is connected the compensation network (Z_C). The maximum positive output voltage is clamped at about 3.5V to improve response time.

The feedback control circuit determines the magamp "off" time, converting the voltage at the output of error amplifier into a current I_R, which resets the magamp. If the output voltage exceeds its preset value, $V(B_{out})$ decreases; this causes a higher voltage across R_C which, in turn, implies a larger voltage across R_E and a larger reset current I_R (V_{BE} of Q_1 is supposed constant). A larger I_R causes the PWM waveform across D_2 to get narrower. This pulls the output voltage back to the desired level and achieves regulation.

It is possible to use this section to drive a pass transistor to obtain 3.3V with a linear regulator; in the "Application idea" section an example is showed to implement this solution.

Figure 16. Magamp control feedback section



– **Auxiliary section, error amplifier C.**

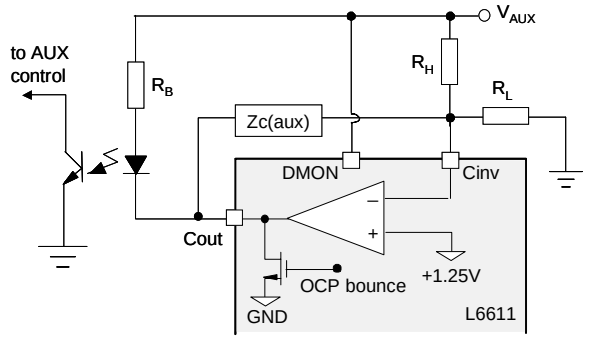
This section (fig. 17) provides the feedback signal for the auxiliary converter following the same operating principles as the Main section. The auxiliary output voltage (Vaux) is often defined as "Standby voltage" because the converter remains alive during standby condition (the Main converter is stopped) to supply the chip and all the ancillary circuits. Typical values for its output voltage are 5V or 3.3V.

The inverting input (Cinv, pin#7) is connected to the output voltage through an external resistor divider whereas the non-inverting one is connected to a 1.25V trimmable internal voltage reference (see "On board trimming and mode operating" paragraph).

The compensation network Zc(aux) is placed between E/A inverting input and output pins.

When Dmon recognizes an undervoltage condition on the auxiliary output, an internal n-channel MOS (in open drain configuration) grounds E/A output pin; the high current flowing through the optocoupler is then transferred to the primary side causing a duty cycle as short as possible; this prevents a high energy transfer from primary to secondary under short circuit conditions, thus reducing the thermal stress on the power components.

Figure 17. Auxiliary feedback section

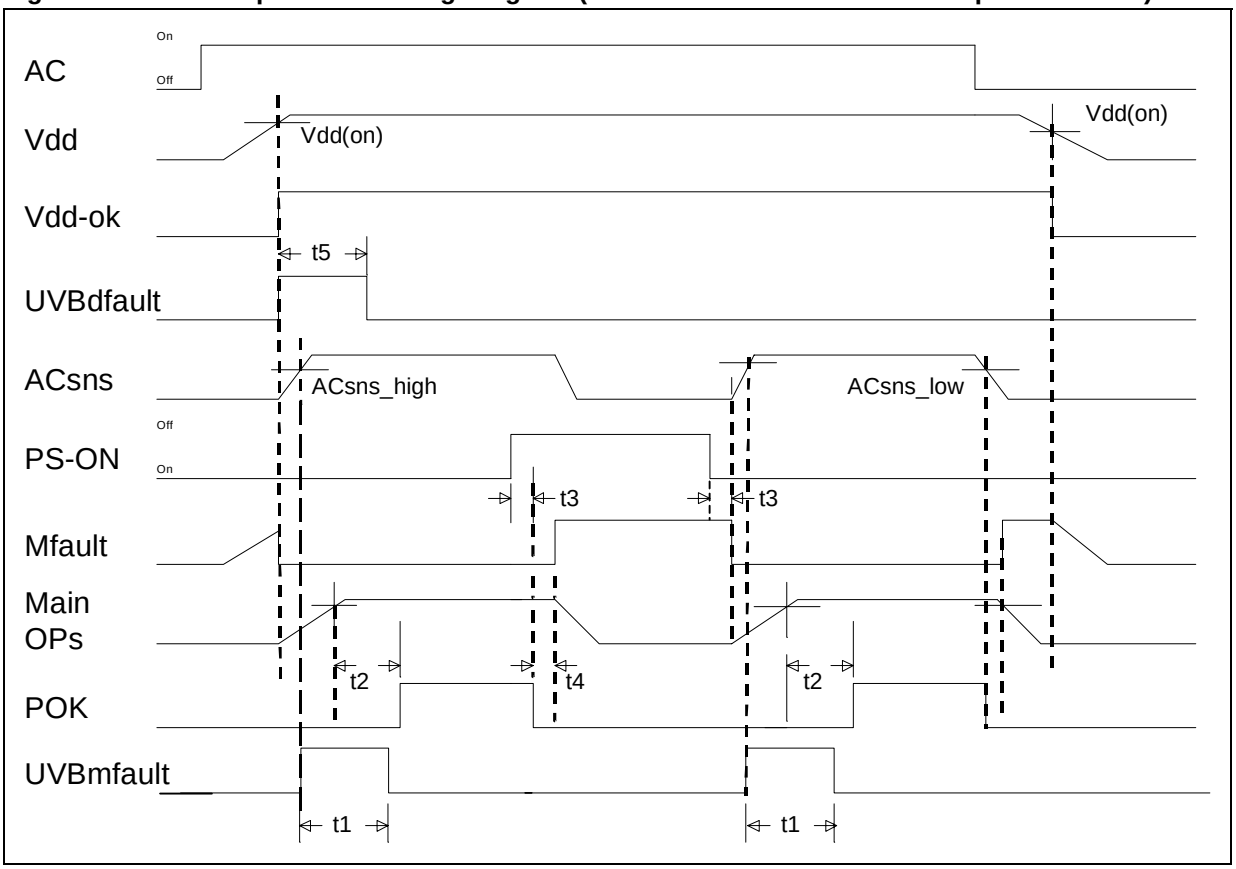


3 NORMAL OPERATION TIMING DIAGRAM (FIG. 18)

The time intervals t1-t5 are listed below

– **t1:** UV/OC blanking of MFAULT. While Main outputs are ramping up, the UV comparators are blanked for this interval to prevent a false turn-off. No such blanking is applied to OV faults.
– **t2:** PW-OK delay. This period starts when all monitored outputs and AC sense are above their respective UV levels and finishes at PW-OK going high.
– **t3:** PS-ON debounce period. The voltage on PS-ON must be continuously present in a high or low state for a minimum period for that state to be recognized.
– **t4:** Tdelay. The time from PS-ON being recognized as going high to MFAULT going high. This is to provide a power down warning. When PS-ON requests power off, PW-OK goes low immediately.
– **t5:** UV blanking of DFAULT. During initial power up a period of UV blanking is applied to DFAULT as soon as Vdd to the chip is in the correct range. No such blanking is applied to OV faults.

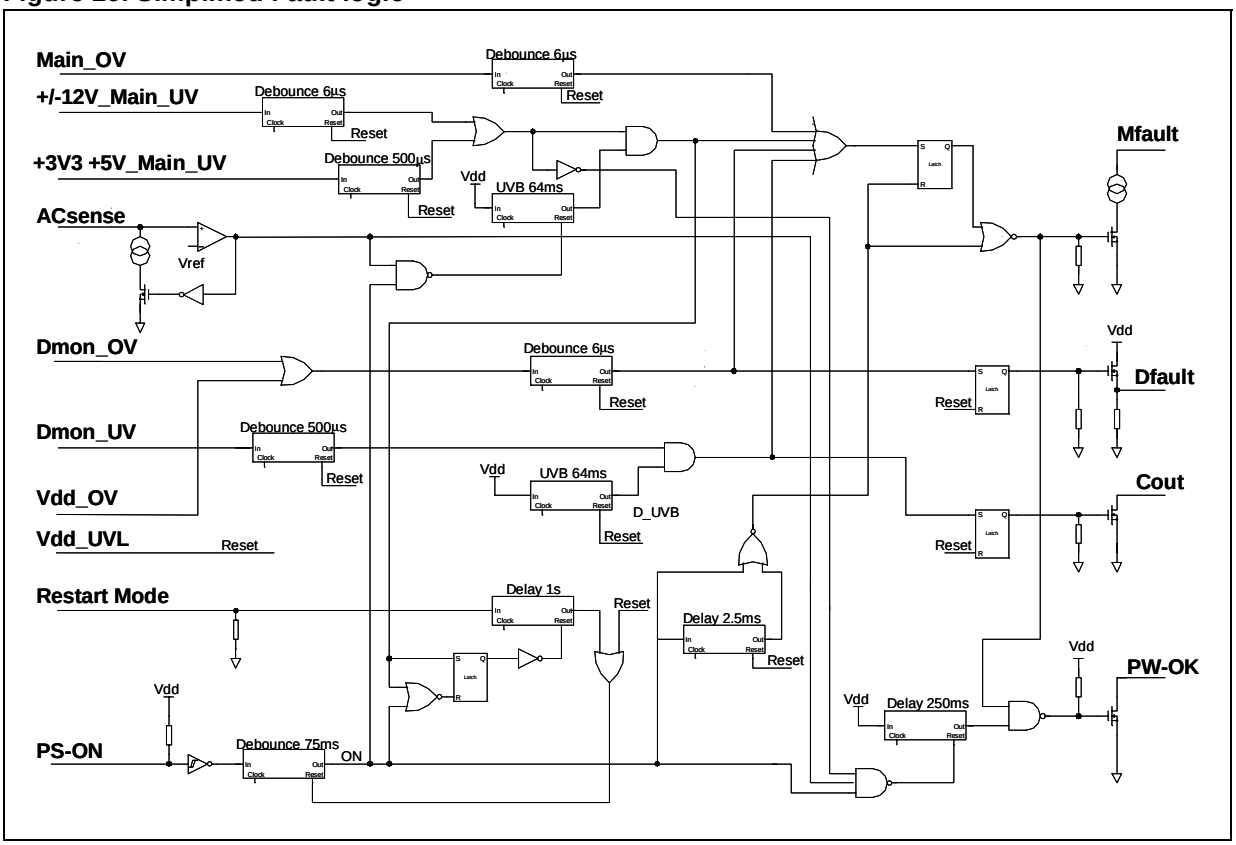
Figure 18. Normal Operation Timing Diagram (ON/OFF with PS-ON or the AC power switch).



4 UNDERVOLTAGE, OVERVOLTAGE, DETECTION AND RELEVANT TIMINGS

The IC provides on-board undervoltage and overvoltage protection for 3V3, ±5V, ±12V Main input pins and Dmon auxiliary input pin. Overcurrent protection is available for 12V and 5V or 3.3V, digitally selectable. The internal fault logic is illustrated in figure 19.

Figure 19. Simplified Fault logic



– **Main inputs overvoltage:** whenever one of main outputs (3.3V, +5V, ±12V) is detected as going overvoltage, MFAULT is latched high (which stops the Main PWM) and PW-OK goes low. Cycling the PS-ON switch or reducing Vdd below its undervoltage threshold releases the latch. A delay of 6µs is implemented before MFAULT latching.
The OV protection for the 12V and 5V outputs can be disabled (see "On board trimming and mode operating" section).

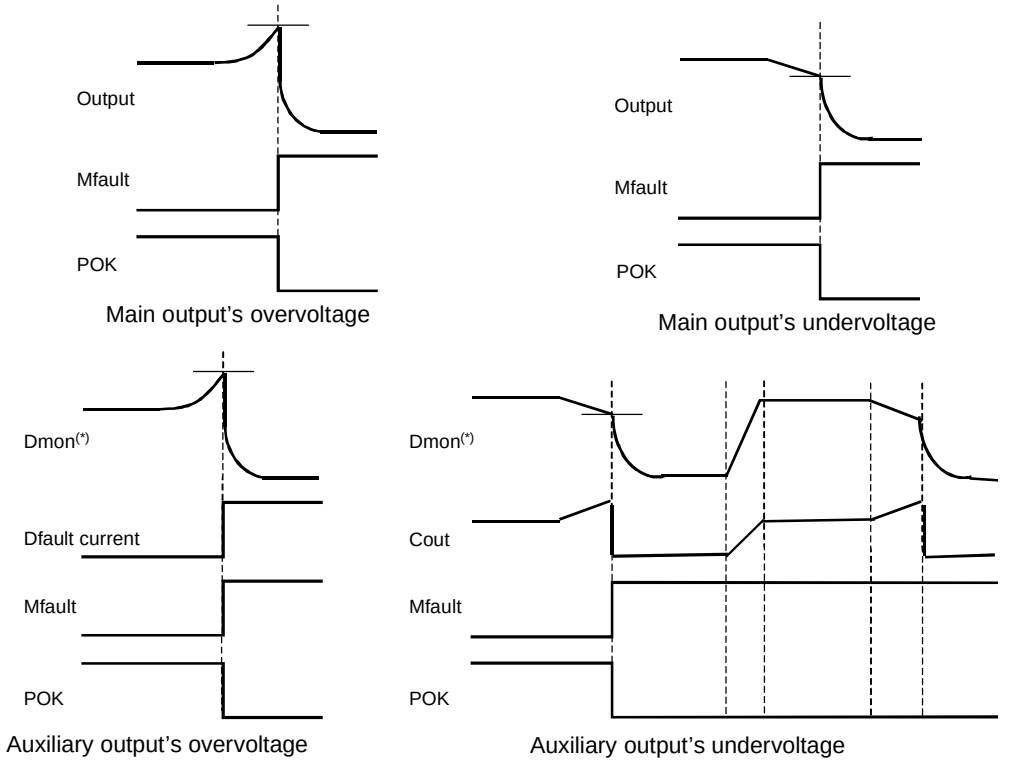
– **Main inputs undervoltage:** when an undervoltage on main outputs is detected, MFAULT is latched high (the Main PWM stops) and PW-OK goes low. The latches are released, by default, cycling the PS-ON switch or reducing Vdd below its undervoltage threshold (latching mode); optionally, an attempt is made to restart the supply after of 1 second (bounce mode). The choice depends on the selected mode (see "On board trimming and mode operating" section).
Debounce logic is implemented for 3.3V and 5V so that an undervoltage condition on these signals has to last 450µs to be recognized as valid while 6µs debounce logic is implemented for 12V and -12V input signal. When all main undervoltages are over and ACsns is OK (see the relevant section), PW_OK goes high after a delay of 250ms.

– **Dmon input overvoltage:** whenever the Dmon input pin is detected as going overvoltage, both MFAULT and DFAULT are latched high. The latch is released by reducing Vdd below its undervoltage threshold. Debounce logic is implemented so that MFAULT and DFAULT signals are latched only if the overvoltage condition lasts more than 6µs.
To protect the load against overvoltage, typical solutions make use of a power crowbar (SCR) driven by

DFAULT; in the "Application ideas" section, another simple circuit is showed to guarantee the same protection without the SCR.

– **Dmon input undervoltage:** when an undervoltage on Dmon is detected, MFAULT is put high, Cout is pulled low (an internal OCP_BOUNCE signal is generated, see fig. 19) and PW_OK falls down. This function is enabled 64ms after the UVLO signal falls down. Debounce logic is implemented so that MFAULT and OCP_BOUNCE signals are generated only if the undervoltage condition lasts more than 500µs.
The Dmon UV and OV protections can be set to work with thresholds set for 5V or 3.3V output voltage: the choice depends on the IC programming.

Figure 20. Fault timing diagram



5 AC SENSE (MAINS UNDERVOLTAGE WARNING)

The device monitors the primary bulk voltage and warns the system when the power is about to be lost pulling down the PW_OK output.

The ACsns pin is typically connected to one of the windings of the main transformer (see fig. 21). Through a single-diode rectification filter, a voltage equal to $V_B = V_{BULK}/N$ (where V_{BULK} is the voltage across the bulk capacitor on primary side and N is the transformer turn ratio) is present at point B. A resistor (R_F) could be useful to clamp voltage spikes present.

The fault signal is generated by means of AC_GOOD, the output of an internal comparator; this comparator is internally referred to a trimmable 2.5V reference and indicates an AC fault if the voltage applied at its externally available (non-inverting) input is below the internal reference, as shown in fig. 21.

This comparator is provided with current hysteresis instead of a more usual voltage hysteresis: an internal 50µA current generator is ON if the voltage is below 2.5V and is turned off when the voltage applied at the non-inverting input exceeds 2.5V.

This approach provides an additional degree of freedom: it is possible to set the ON threshold and the OFF

threshold separately by properly choosing the resistors of the external divider. The following relationships can be established for the ON ($VB_{(ON)}$) and OFF ($VB_{(OFF)}$) thresholds of the input voltage:

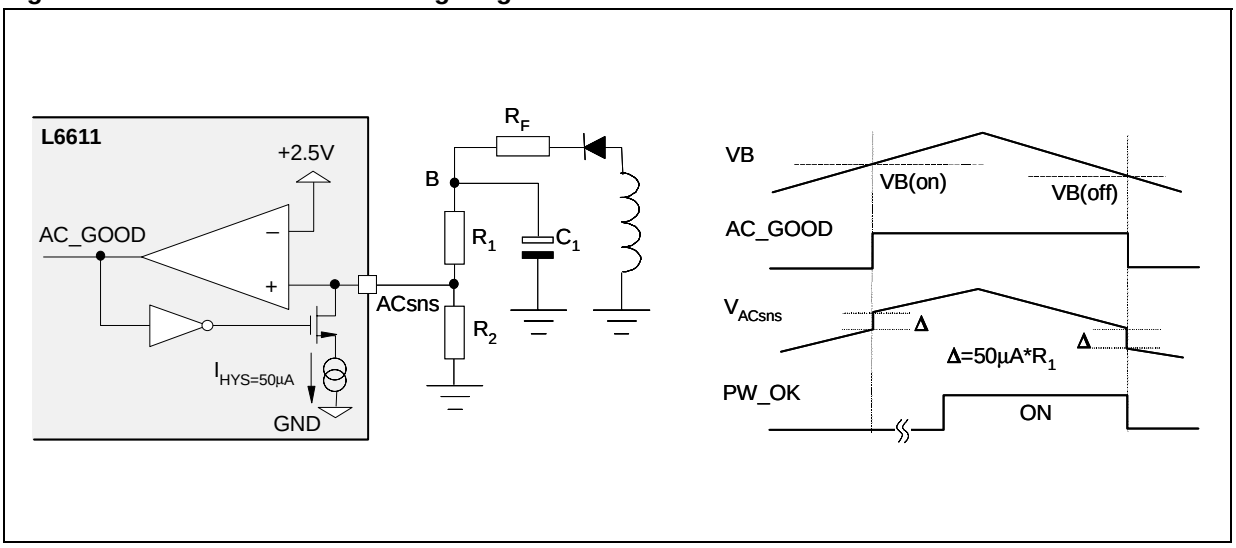
$$\frac{VB_{(ON)} - 2.5}{R_1} = \frac{2.5}{R_2} + 50\mu A \qquad VB_{(OFF)} \cdot \frac{R_2}{R_1 + R_2} = 2.5$$

which, solved for R1 and R2, yields:

$$R_1 = \frac{VB_{(ON)} - VB_{(OFF)}}{50\mu A} \qquad R_2 = R_1 \cdot \frac{2.5}{VB_{(OFF)} - 2.5}$$

Both the ACsns threshold and the hysteresis current can be trimmed (see "On board trimming and mode operating" section).

Figure 21. ACsns circuit and timing diagram



6 APPLICATION EXAMPLE

In applications like desktop PC's, server or web server, the system usually consists of two converters (Main and Auxiliary) that can be supplied directly from either the AC Mains or a PFC stage. The control and supervision at the secondary side is usually entrusted to a housekeeping circuit.

The Auxiliary section supplies a stand-by voltage (5V typ.) through a flyback converter. The Main section, in forward configuration, presents 4 standard outputs (3.3V, +5V, ±12V).

At the secondary side, the housekeeping circuitry governed by the L6611 checks the outputs and sends control signals to the primary side through three optocouplers. It also generates power good information to the system while managing all timings during power-up and power-down sequences. In fig. 22 a detailed circuit for the secondary side is presented; it is possible to note the very low number of external components required.

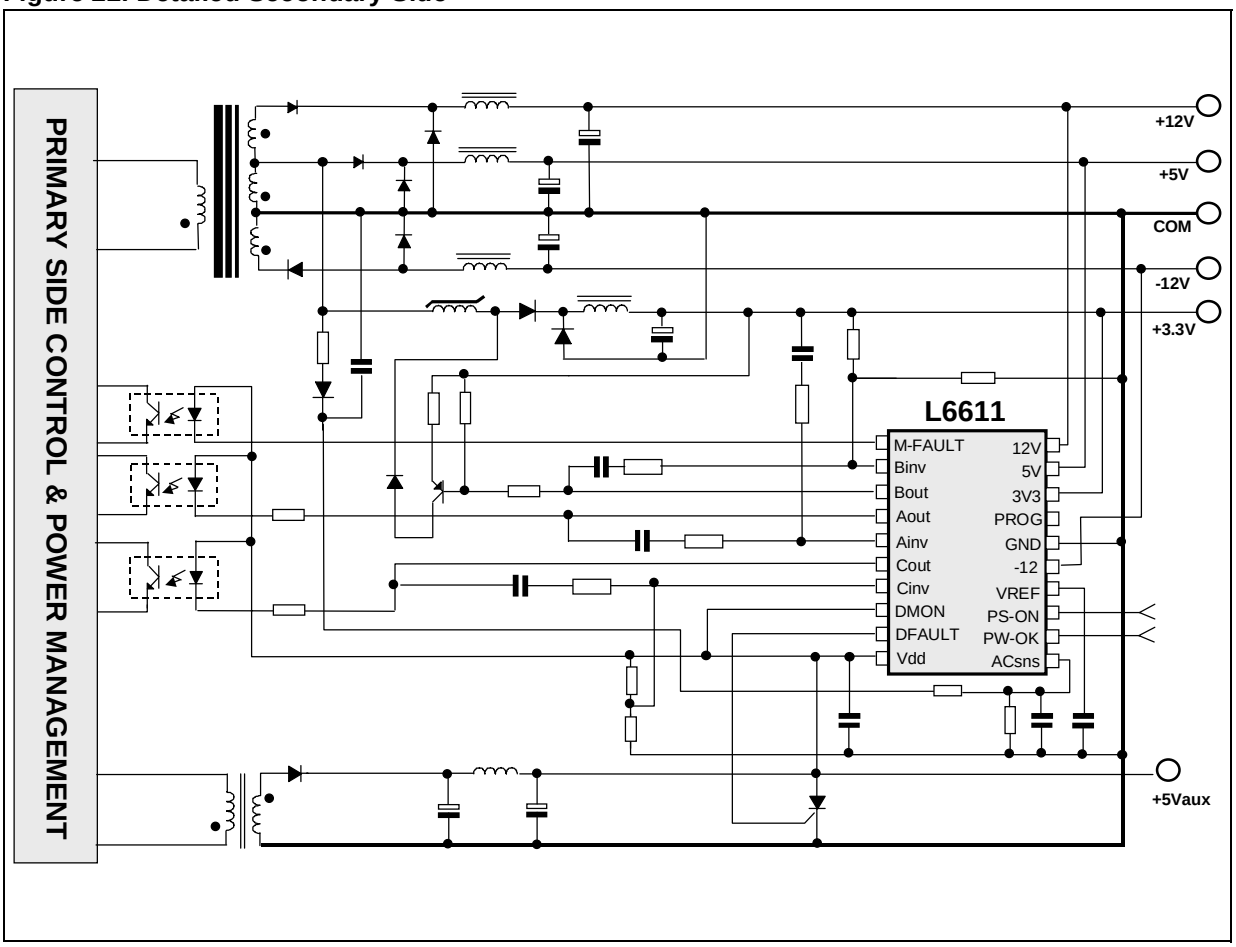
Simply connecting the power supply outputs to the L6611 relevant pins ensures the protection against over/undervoltage in the Main section.

A crowbar on the auxiliary output is switched on through DFAULT in case of overvoltage.

The L6611 is supplied by the Auxiliary output; the signals sent to the primary side are:

– a "digital" ON/OFF signal through an optocoupler that drives the relevant pin of primary Main controller to switch the Main converter ON and OFF;
– two analog signals that provide voltage feedback for both the Auxiliary and the Main section, driving the primary controller pins responsible for the duty cycle modulation.

Figure 22. Detailed Secondary Side



7 APPLICATION IDEAS

In fig. 23 a circuit is suggested to obtain the regulated +3.3V output with a linear configuration instead of the Magamp circuitry.

In this case the output of the E/A modulates the gate-source voltage of a power MOS in series with the power stage.

In fig. 24 a simple and cheap latch circuit is showed to manage an OV fault on the Auxiliary output in the same way of an OC (UV) fault, without having recourse to a (expensive) power crowbar. By tuning the value of R_{SET} it is possible to set the voltage value that triggers the latch circuit; C_{DEL} defines the turn-on delay. A diode connected between the collector of Q1 and Cout pulls down the output of the auxiliary E/A: this has the same effect of the OCP_bounce internal signal that guarantees the reduction of duty cycle.

Figure 23. Controlling a Linear Regulator with the Error Amplifier B

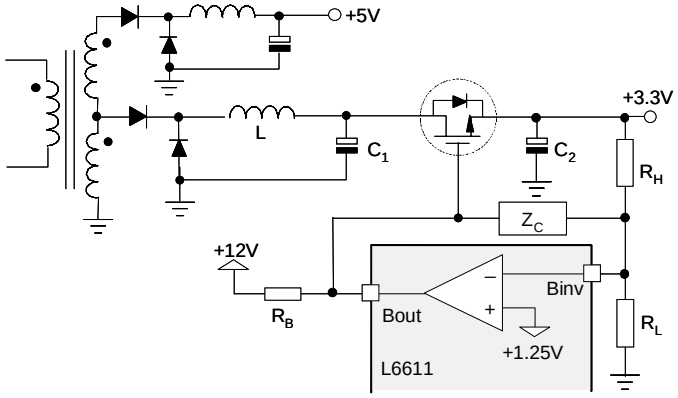
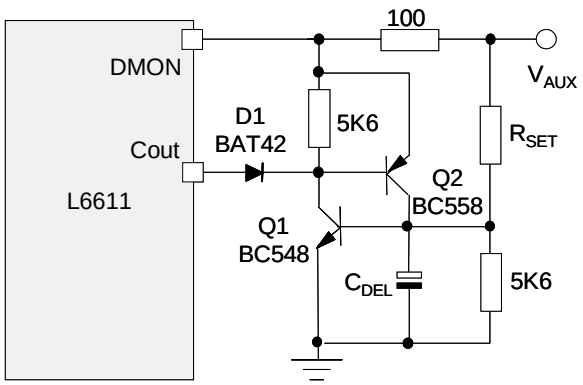
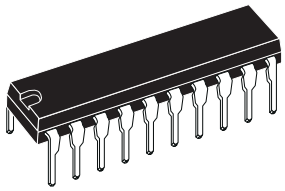


Figure 24. Auxiliary OVP without Crowbar

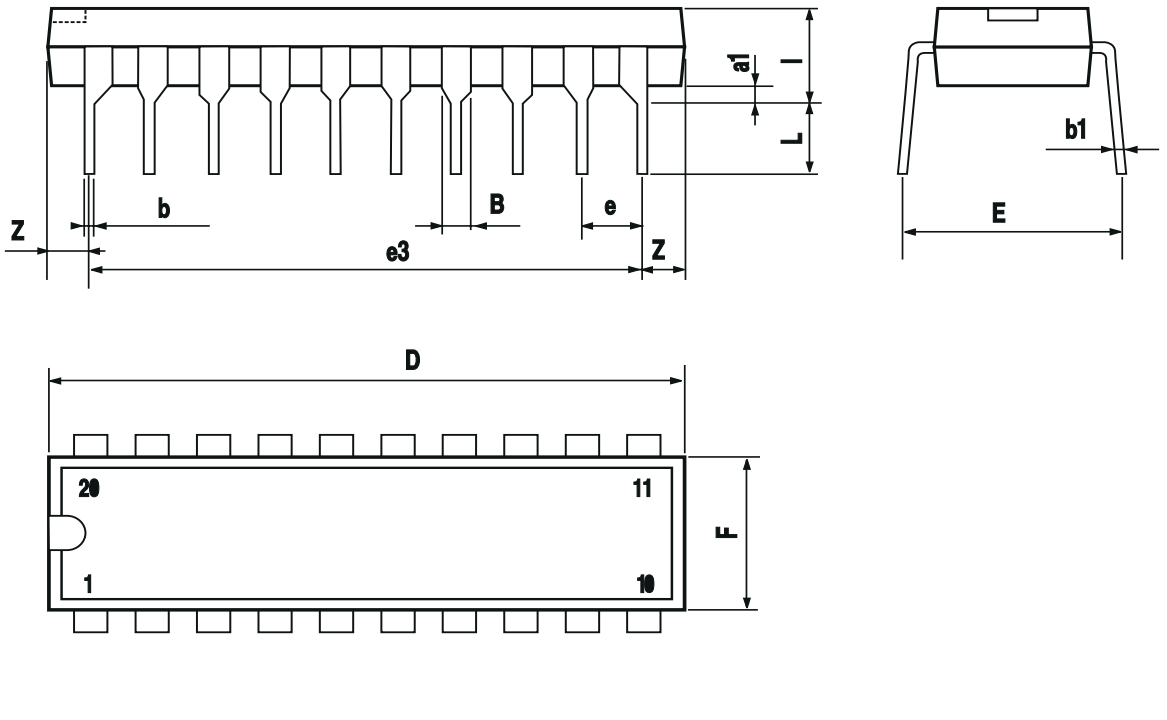


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

OUTLINE AND MECHANICAL DATA

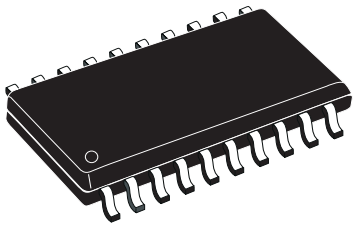


DIP20

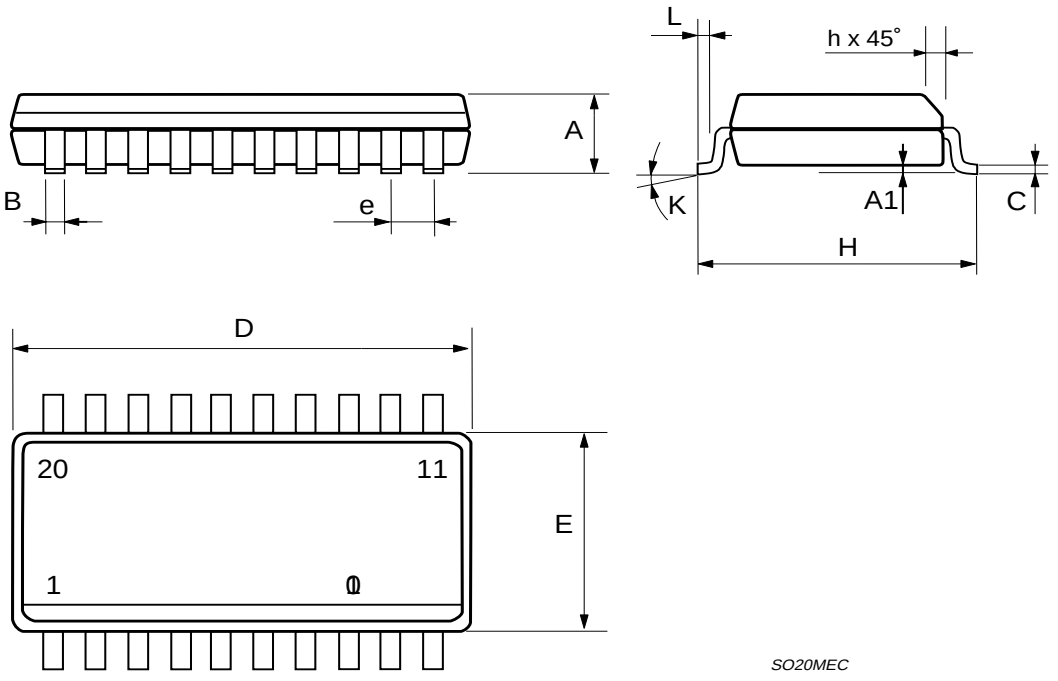


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0˚ (min.)8˚ (max.)					

OUTLINE AND MECHANICAL DATA



SO20



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